# High Accuracy printed electronics down to µm size, for Organic Large Area Electronics (OLAE) Thin Film Transistor (TFT) and Display Applications

**H2020- DT-NMBP-18-2019**

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## PUBLIC SUMMARY OF Deliverable Report: D6.3 Fabrication of flexible test structures for testing of ESJET/ROP electrode, pixel-defining layer and encapsulation including public summary

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**Type: Public (PU)**

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| Dissemination level | | |
|---|---|---|
| **PU** | Public | **X** |
| **CO** | Confidential, only for members of the consortium (including the Commission Services) | |

# 1 PUBLIC SUMMARY

In Hi-Accuracy, pixel test structures are functional intermediate devices for the development of materials and printing processes on the way to the fully printed demonstrator in WP7. In WP6, the focus is on front-plane layers. Previous deliverables in WP6 have described the design of pixel test structues(Del 6.1) and the fabrication of rigid pixel test structures for QD performance testing, (Del 6.2) the latter including a public summary. Del 6.3 is focused on flexible pixel test structures and of multiple interest in Hi-Accuracy:

1. To develop and demonstrate printing technologies for a structured QD-LED metal electrode
2. To develop and demonstrate printing technologies for the pixel defining layer
3. To use the pixel test structures for printing fully functional flexible QD-LEDs without backplane (Del. 6.5) as test samples to the final demonstrator in WP7
4. To test bendability and performance of printed pixel electrode, pixel defining layer and QD-LED
5. To test ALD top encapsulation for flexible ESJET printed devices (D6.5)

During the planning of materials and processes in WP1 it has been concluded, that silver is a suitable electrode material for the QD-LED electrode as long as the cured layer is free of spikes (>20 nm) and exhibits an RMS roughness $R_q$ below 10 nm. PVI has developed ESJET printing processes using Dycotec silver ink with good printability as demonstrated for printing on paper (Figure 1).

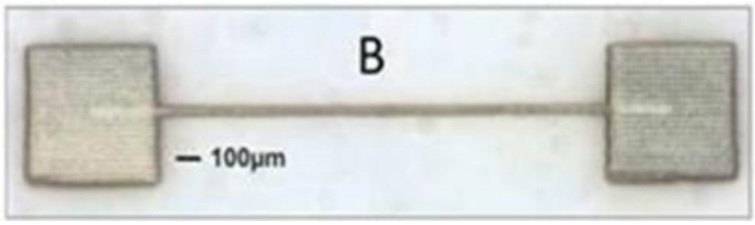


*Figure 1: Test structure for pixel electrode printed by PVI with ESJET using Dycotec silver Ink on paper. Pixels were printed with 50% overlap and a pitch of 10 mm to create a wire.*

For the pixel defining layer, a homogeneous dielectric layer with small openings (cavities) has to be created, i.e. the negative image has to be printed. In WP1 it has been concluded that a strong wetting contrast is required between the bank structure (dewetting or high contact angle) and the pixel electrode (wetting or low contact angle). It is envisioned, that the printed QD-LED stack layers as ESJET printed onto the pixel electrodes will distribute evenly across the whole electrode, whilest not spreading across the adjacient pixel defining layers. Including lessons learned from rigid pixel test structures manufactured by ND using photolithography, the polymer Cytop™ was chosen. Cytop™ is amongst the most dewetting laquers available.

However printing trials using ROP and ESJET did not prove successful in printing the pixel defining layer. Hence PVI developed its novel technology of High-Resolution Screen Stencil Mesh printing (HRSSM) further in order to print the pixel defining layer. It could be shown, that tailor-made stencil foils can be structured in the range of only a few µm by laser ablation and

used for high-resolution prints of dielectrics (Figure 2, achieved resolution so far: below 20 µm).

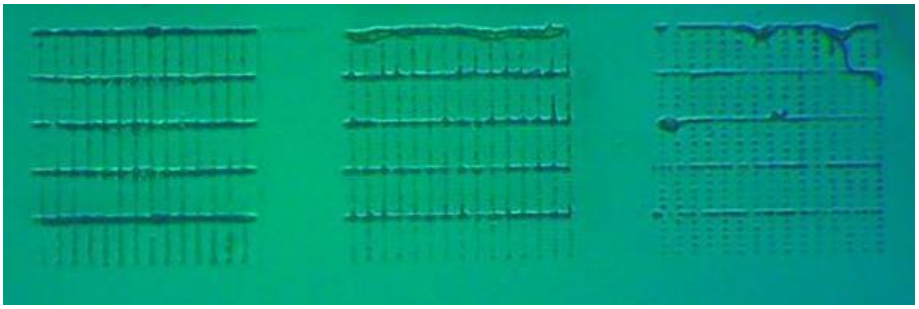

*Figure 2: Test prints of high-wetting dielectric ink on glass substrate using HRSSM and a 12 µm Kapton film stencil (hole size: 3 - 8 µm, pitch: 7 - 14 µm)*

Both, the ESJET printing of pixel electrodes and HRSSM printing of bank structrues are both behind schedule with further developments required. That is the reason why ND processed flexible test structures by photolithography using the same layout as developed in Del. 6.1 and 6.2. Here, the challenge was to use the stronger dewetting dielectric Cytop™ as compared to the ND-P11 before, which required further optimizations in the process. Finally a flexible pixel test structure could be manufactured and delivered to Fraunhofer IAP for further testing (Figure 3).

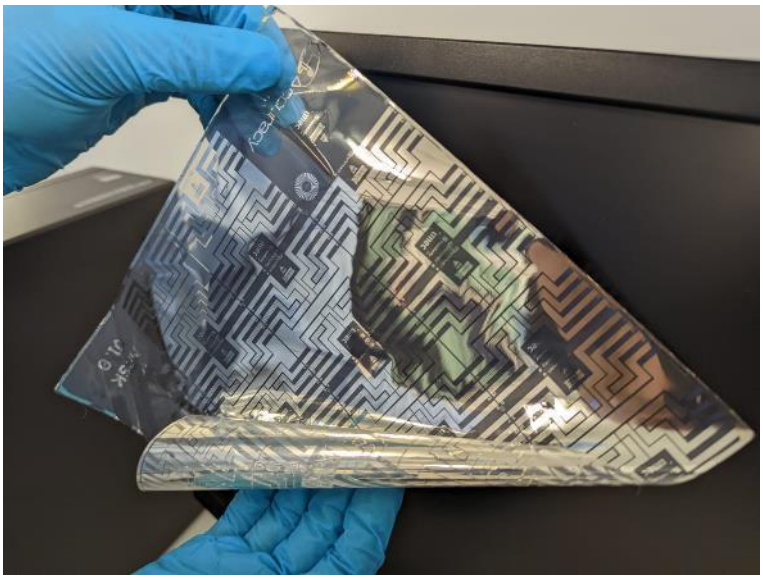

*Figure 3: Flexible pixel test structure made by ND on PEN foil using photolithographic structuring of Cytop™*

Despite showing strong progress in process development, those flexible pixel test structures are not suitable for the intended tests for D6.5. The reason is twofold: First, the intended foils supplied from ND and coated with ALD barriers at Fraunhofer IAP were stuck in customs for 3 months and arrived too late at ND. Hence, those pixel test structues do not exhibit any ultra-high wvtr barrier. Second, the process was done on foils without planarization layer, yielding spikes of more than 150 nm in height (Figure 4).

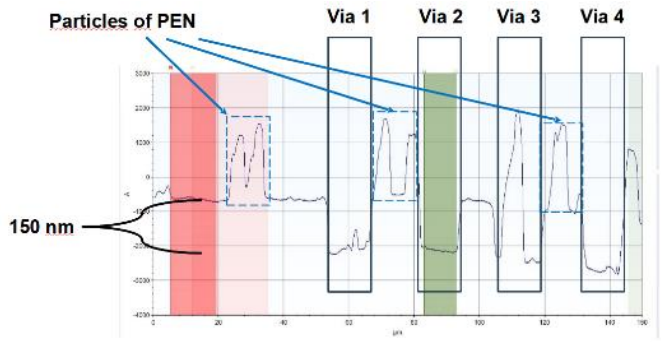


*Figure 4: Dektak profilometric measurement on flexible pixel test structures demonstrating a Cytop™ layer thickness of ~150 nm, but also particles on the PEN foil of similar heights.*

In the following project, PVI will develop its HRSSM process further with the aim to deliver fully printed pixel test structures later in the project. Additionally a new batch of flexible pixel test structures processed by photolithography is envisaged.